

FORM PTO-1390
(REV. 11-2000)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER

20496-301

TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)
CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)

09/914687

INTERNATIONAL APPLICATION NO.
PCT/EP00/01705INTERNATIONAL FILING DATE
1 March 2000PRIORITY DATE CLAIMED
4 March 1999

TITLE OF INVENTION

IMAGE SENSOR

APPLICANT(S) FOR DO/EO/US

Markus BOHM

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 - a. ☐ is attached hereto (required only if not communicated by the International Bureau).
 - b. ☒ has been communicated by the International Bureau.
 - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
 - a. ☒ is attached hereto.
 - b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
 - a. ☐ are attached hereto (required only if not communicated by the International Bureau).
 - b. ☐ have been communicated by the International Bureau.
 - c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
 - d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
14. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information:
 - 1) Express Mail Mailing Label No. EL070211633US

U.S. APPLICATION NO. (if known, see 37 CFR 1.55)

09/914687

INTERNATIONAL APPLICATION NO
PCT/EP00/01705ATTORNEY'S DOCKET NUMBER
20496-30121. ☒ The following fees are submitted:**BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):**Neither international preliminary examination fee (37 CFR 1.482)
nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO
and International Search Report not prepared by the EPO or JPO. \$1000.00International preliminary examination fee (37 CFR 1.482) not paid to
USPTO but International Search Report prepared by the EPO or JPO \$860.00International preliminary examination fee (37 CFR 1.482) not paid to USPTO
but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$710.00International preliminary examination fee (37 CFR 1.482) paid to USPTO
but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$690.00International preliminary examination fee (37 CFR 1.482) paid to USPTO
and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00**ENTER APPROPRIATE BASIC FEE AMOUNT =**

CALCULATIONS PTO USE ONLY

\$ 860.00

Surcharge of \$130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30
months from the earliest claimed priority date (37 CFR 1.492(e)).

\$

CLAIMS

NUMBER FILED

NUMBER EXTRA

RATE

\$

Total claims

23 - 20 =

3

x \$18.00

\$

54

Independent claims

1 - 3 =

0

x \$80.00

\$

0

MULTIPLE DEPENDENT CLAIM(S) (if applicable)

+ \$270.00

\$

0

TOTAL OF ABOVE CALCULATIONS =

\$ 914.00

☒ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above
are reduced by 1/2.

\$

-457.00

SUBTOTAL =

\$ 457.00

Processing fee of \$130.00 for furnishing the English translation later than ☐ 20 ☐ 30
months from the earliest claimed priority date (37 CFR 1.492(f)).

\$

TOTAL NATIONAL FEE =

\$ 457.00

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be
accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +

\$

TOTAL FEES ENCLOSED =

\$ 457.00

Amount to be
refunded:

\$

charged:

\$

- a. ☐ A check in the amount of \$ _____ to cover the above fees is enclosed.
- b. ☒ Please charge my Deposit Account No. 16-2500 in the amount of \$ 457.00 to cover the above fees.
A duplicate copy of this sheet is enclosed.
- c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any
overpayment to Deposit Account No. 16-2500. A duplicate copy of this sheet is enclosed.
- d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card
information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR
1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

Charles Guttman

NAME

Reg. No. 29,161

REGISTRATION NUMBER

09/914687

422 Rec'd PCT/PTO 3 1 AUG 2001

Attorney Docket No. 20496-301

IN THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

Patent Application of	:	Markus BOHM
Int'l Appl. No.	:	PCT/EP00/01705
Int'l Filing Date	:	1 March 2000
Priority Date	:	4 March 1999
Title of the Invention	:	IMAGE SENSOR

**PRELIMINARY
AMENDMENT**

"Express Mail" mailing label number <u>EL070211633US</u>

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified patent application as follows:

IN THE SPECIFICATION:

Page 1, after the title, please insert --BACKGROUND OF THE INVENTION--.

Page 3, before the third paragraph, which begins with "The invention is distinguished," please insert
--SUMMARY OF THE INVENTION--.

Page 5, before the last paragraph, which begins with "The invention will be further," please insert
--BRIEF DESCRIPTION OF THE DRAWINGS--.

Page 6, before the paragraph, which begins with "Fig. 1 shows," please insert --DETAILED
DESCRIPTION OF THE INVENTION--.

IN THE CLAIMS:

Please amend claims 1 and 23 as follows. Also please amend claims 16 and 22 to remove their multiple dependencies. A "marked-up" version of the amended claims is enclosed herewith in accordance with 37 C.F.R. 1.121 (c)(1).

--1. (Amended) An image sensor consisting of a semiconductive carrier (substrate) (1), especially in a CMOS design, on which an arrangement of pixels is placed, and each pixel is assigned a photosensitive detector (4), means to photoelectrically convert a detected photosignal into an electrical signal, and electrical storage means (3) to store the electrical signal, whereby a storage control device (2) is provided to store the electrical signals related to each pixel and read them out in a controlled manner, characterized in that for storing of a number of pictures, in the way of an electronic film, a number of storing means ($C_1 \dots, C_N$) is provided in a single pixel, the number of which storing means corresponding to the number pictures to be stored and that the storage for the first picture to be recorded control device (2) is operating so that the image information of the first picture is read into a first one of the storage means and that for each of the subsequent pictures to be recorded the image information allocated to the corresponding pixel is read into one of the other storage means, respectively, until finally all storage means ($C_1 \dots, C_N$) are filled up.

--16. (Amended) An image sensor according to claim 1, characterized in that the storage (3) is operated using a multilevel digital approach in which numerous digital bits are represented in an amplitude-discretized analog signal.

--22. (Amended) An image sensor according to claim 1, characterized in that the storage control (2) is on the surface of the carrier (1) designed as CMOS substrate.

--23. (Amended) An image sensor according to claim 1, characterized in that the electrical storage (3) is in a layer between the carrier (1) and the detector (4), and the connection between the storage (3) and storage control (2) is provided by via holes (6).

IN THE ABSTRACT:

Please delete the last line, which begins with "Fig. 1 is provided."

REMARKS

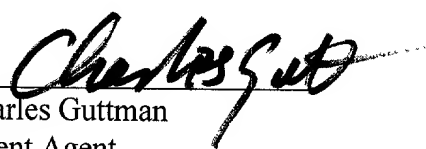
Amendments are being made to claims 16 and 22 to remove their multiple dependencies.

Please proceed to examine the application as amended herein.

Respectfully submitted,
PROSKAUER ROSE LLP
Attorneys for Applicant(s)

Date: August 31, 2001

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New York, NY 10036
Tel: (212) 969-3000

By 
Charles Guttman
Patent Agent
Reg. No. 29,161

Amended Claim - Marked-Up Version

--3. (Amended) An image sensor consisting of a semiconductive carrier (substrate) (1), especially in a CMOS design, on which an arrangement of pixels is placed, and each pixel is assigned a photosensitive detector (4), means to photoelectrically convert a detected photosignal into an electrical signal, and electrical storage means (3) to store the electrical signal, whereby a storage control device (2) is provided to store the electrical signals related to each pixel and read them out in a controlled manner, characterized in that [the storage control (2) is designed so that, in a single pixel, sequentially-recorded, photoelectrically-transformed signals can be stored in different storage means (3) and they can be read out of the storage means (3) at a given time.] for storing of a number of pictures, in the way of an electronic film, a number of storing means (C_1 ..., C_N) is provided in a single pixel, the number of which storing means corresponding to the number pictures to be stored and that the storage for the first picture to be recorded control device (2) is operating so that the image information of the first picture is read into a first one of the storage means and that for each of the subsequent pictures to be recorded the image information allocated to the corresponding pixel is read into one of the other storage means, respectively, until finally all storage means (C_1 ..., C_N) are filled up.

--16. (Amended) An image sensor according to [one of the prior claims] claim 1, characterized in that the storage (3) is operated using a multilevel digital approach in which numerous digital bits are represented in an amplitude-discretized analog signal.

--22. (Amended) An image sensor according to [one of the prior claims] claim 1, characterized in that the storage control (2) is on the surface of the carrier (1) designed as CMOS substrate.

--23. (Amended) An image sensor according to claim [23] 1, characterized in that the electrical storage (3) is in a layer between the carrier (1) and the detector (4), and the connection between the storage (3) and storage control (2) is provided by via holes (6).

4/PRTS

09/914687
422 Rec'd PCT/PTO 31 AUG 2001

IMAGE SENSOR

The invention concerns an image sensor consisting of a semiconductive carrier (substrate), especially one constructed using CMOS technology, on which an arrangement of picture elements is created. Each picture element (pixel) is assigned a photosensitive detector, means to photoelectrically convert a detected photosignal into an electrical signal, and electrical storage means to store the electrical signals. A storage control device is provided to store the electrical signals related to each pixel and read them out in a controlled manner.

A prior-art device of the type cited above is in WO 98/19455, i.e., PCT/EP97/05978. This is an optical image sensor, e.g. for use in a camera in which each pixel can record all the color information in each picture sequence depending on the incident light and can supply the information in electronic form. Each pixel of the sensor structure organized in a matrix has several information stores to simultaneously buffer the different color information. In addition, the sensor contains controllable detector elements whose spectral sensitivity can be changed.

There are state-of-the-art image sensors with different designs in the form of CCD image sensors, e.g. „CCD-CMOS Image Sensor for Ultra-High Speed Image Capturing“ in 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 10-12, 1999, Karuizawa, Nagano, Japan, p. 99 - 102.

Another prior-art image sensor arrangement is found in „A Passive Photodiode Pixel with Memory“ in 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 10-12, 1999, Karuizawa, Nagano, Japan, p. 84 - 87 that develops a conventional passive photosensor by proposing a charge store in the form of a separate capacitor.

There are prior-art photoelectric sensor devices used for digital cameras that are designed in the form of three chips: an image sensor, a store and the assigned storage control device (controller). This solution accordingly has three separate chips.

In another variation of the sensor device for digital cameras, the storage arrangement is on the same chip with the corresponding store control outside of the sensor surface.

When they are used for digital cameras, the measured values (recorded by the sensor and transformed into electrical signals) of the prior-art devices must be read out directly after each picture is taken, normally using a prior-art compression process such as JPEG, and the measured values are stored in an external storage device. The sensor is ready for the next picture only after these steps have been accomplished.

A disadvantage of the conventional sensor is hence that extremely fast picture sequences are not possible due to the transfer times required by the readout procedure. If the storage and image sensor are both in one chip, the storage takes up a large part of the entire chip surface.

Given these facts, the invention is based on the problem of developing an image sensor of the type cited at the onset so that the area of the chip is used more effectively, and the image sensor can be used in a high-speed camera.

This problem is solved according to the invention by designing the storage control device so that in a single pixel the sequentially-recorded photoelectrically transformed signals can be stored in different storage means and they can be read out of the storage means at a given time.

The invention is distinguished in that the image sensor device allows several pictures to be taken sequentially like an „electronic film“ without the image information having to be read out in between. The several storage means assigned to each pixel (controlled by the storage controller) allow the sequential pictures to be saved in the respective storage means. After taking all the pictures of the „film,“ the corresponding storage values can then be quickly read out and reproduced independent of the picture-taking process. The length of storage only depends on the physical transitory nature of the information. Otherwise the read-out time can be freely selected by the user. For example, 36 black/white pictures or 24 color pictures (depending on the used black/white or color detector) can be stored. This allows the pictures to be taken in ultrafast succession by high-speed cameras.

Another advantage of the solution according to the invention is that the sensor surface is used more

effectively since no additional or separate space is required on the image sensor surface for the storage. The storage means are arranged pixel-wise in the detector since the individual storage cells are directly above or next to the detector or inside it. The arrangement according to the invention unites the detector and storage matrix on the pixel level.

Preferred embodiments of the invention are found in the subclaims:

Photodetectors made of crystalline silicon or amorphous silicon can be used as the detector means, and they can also be made of III-V alloys, II-VI alloys, or an organic or any other detector device to transform light into an electrical signal. The used sensors can be sensitive to visible light, UV light, IR light, X-rays or any other ray that can be transformed into an electrical signal.

An advantageous development of the device allows numerous color pictures to be stored, e.g. by applying color filter arrays as e.g. are conventional in color CCD technology, or by using a multispectral diode as is described in the state-of-the-art in PCT/EP/97/05978.

The storage means can save the electrical signals either as an analog or digital representation, or also in mixed form as e.g. in multilevel digital technology in which several digital bits are represented in an amplitude-discretized analog signal. In order to save the signal as a digital representation, each pixel contains an analog-digital conversion device such as a single-slope, dual-slope, cyclic-pipeline or sigma-delta A/D converter.

Another advantageous development of the device uses a reciprocal A/D converter that does not directly digitalize the intensity of the electrical signal but rather measures the time that the signal requires to attain a specific effect, i.e., the time (for example) that the illumination-proportional photostream requires to recharge a capacitor a specific voltage difference.

Whether analog or digital, the storage means can be laterally adjacent or vertically integrated, or both means of integration can be used. Vertical integration is also termed 3D integration and uses the third dimension to increase the attainable number and density of electrical elements on a given surface.

In another advantageous embodiment in which the storage means are vertically integrated, there are other electrically-active components in the same vertical plane such as transistors that are needed either to store and/or read out the information from the storage means.

The storage means can be designed as capacitors or as EPROM, EEPROM or DRAM cells independent of whether analog or digital signals are to be stored. Digital signals can also be stored in SRAM cells. Magnetic, optical, organic, biological or any other kind of storage cell can also be used. If electrical capacitors are used, trench or planar capacitors are prior-art, advantageous designs.

The invention will be further explained in the following using drawings of exemplary embodiments. Shown are:

Fig. 1 A first exemplary embodiment of an image sensor device according to the invention,

Fig. 2 A second exemplary embodiment of an image sensor device according to the invention,

Fig. 3 A third exemplary embodiment of an image sensor device according to the invention,

Fig. 4 A circuit diagram to clarify the operation of an image sensor device according to the invention.

Fig. 1 shows an image sensor device that is the subject of the first exemplary embodiment of the invention. The arrangement consists of a substrate 1 serving as a carrier that is in a conventional CMOS design. Integrated in the surface of substrate 1 is an electronic circuit device 2 that serves to control the electronic storage arrangement described below. On the surface of the substrate 1, a storage layer 5 has been deposited on whose surface a detector layer 4 is placed. The bottom side of the detector layer 4 is connected by a via hole 6 to the electronic control device 2. In the storage level 5 are several separate electrical storage means 3 that are also connected to the control device 2 by other vias 10. The several storage means C1, C2, CN are designed as plate capacitors.

The drawing in Fig. 1 shows the delimitation of an individual pixel between two vertical lines, i.e., the formed distance precisely corresponds to one pixel. The operation of the device according to the invention is as follows: The picture that is taken falls from above onto

the detector layer 4, and the image information corresponding to the observed pixel is photoelectrically transformed and read into the first storage C1 as electrical information. The read-in procedure is controlled by the pixel electronics 2 acting as a storage control. When the next picture is taken, the storage control 2 causes the image information (transformed into an electrical signal) falling on the pixel to be read into the second storage means C2, etc. until all storage means C1 - CM are filled, and their number corresponds to the maximum number of pictures that can be taken.

After the pictures are taken, the individual storage values C1, C2, CN are read out of the storage cells into an additional storage (not shown) from which the image information undergoes further processing; in particular, the overall picture is assembled. The particular advantage is that the image information is stored uniformly pixel by pixel, and the individual pictures can be later reconstructed from it. Since there are no respective read-out processes directly after the individual pictures are taken, heretofore unheard of picture-taking speeds can be attained.

Overall, the corresponding arrangement of the pixels on the surface of the image sensor and the organization of the storage control arrangement serves the function of an "electronic film".

The second exemplary embodiment of the invention in Fig. 2 differs from the drawing in Fig. 1 in that the detector 4 is directly above the substrate 1 in a layer system, and it is connected by the via hole layer 6 to the pixel

electronics 2 acting as the storage control unit. The numerous storage elements 3 that are assigned to the individual pixels delimited by the vertical lines are arranged in the same horizontal plane as the pixel control 2.

The third exemplary embodiment in Fig. 3 is characterized in that the CMOS substrate 1 has the memory control electronics 2 and the numerous storage elements 3 as well as the detector device 4 in a common horizontal plane. The detector device 4 is designed as a photodiode. In this arrangement, the vias as in Fig. 1 and 2 can be dispensed with.

The detector layer 4 can alternatively be designed as a simple photodiode as well as a photodiode with a color filter array, or as a multispectral diode as is further described in the state-of-the-art in WO 98/19455.

Fig. 4 shows an exemplary electronic circuit that is used to control the image sensor in one of the exemplary embodiments 1 - 3. The photostream provided by the detector is converted by means of the inverter M4, M5 / capacitor Ci combination into a voltage proportional to the photostream (see WO 98/19455, i.e., PCT/EP97/05978). Simultaneously, the inverter provides a constant potential at the detector cathode K.

The integration time starts after activating „int“ and deactivating the „reset“ signal, and the picture information is stored as a voltage value in one of the pixels selected by Pic0...Pic3 and connected to Cp0...Cp3. The picture taking is terminated by

deactivating „int.“ After a brief reset phase, another picture can be taken by selecting another storage without reading out the prior picture. After filling all the storages (in the example, the four storage elements corresponding to terminals Cp0...Cp3), the signal „read_int“ is activated by means of driver stage M10, and the stored pictures can be successively read out by activating the corresponding control signals Pic0...Pic3.

CLAIMS

1. An image sensor consisting of a semiconductive carrier (substrate) (1), especially in a CMOS design, on which an arrangement of pixels is placed, and each pixel is assigned a photosensitive detector (4), to photoelectrically convert a detected photosignal into an electrical signal, and electrical storage means (3) to store the electrical signal, whereby a storage control device (2) is provided to store the electrical signals related to each pixel and read them out in a controlled manner, characterized in that the storage control (2) is designed so that, in a single pixel, sequentially-recorded, photoelectrically-transformed signals can be stored in different storage means (3) and they can be read out of the storage means (3) at a given time.
2. An image sensor according to claim 1, characterized in that the image sensor has a linear arrangement of pixels.
3. An image sensor according to claim 1, characterized in that the image sensor has a flat arrangement of pixels.
4. An image sensor according to claim 1, characterized in that the detector (4) is a photodiode, especially made of crystalline or amorphous silicon.

5. An image sensor according to claim 1, characterized in that the detector (4) is a photodetector made of a III-V alloy or a II-IV alloy.
6. An image sensor according to claim 1, characterized in that the detector (4) has a color filter array.
7. An image sensor according to claim 1, characterized in that the detector (4) is a multispectral diode that has the following sequence of layers:
 - (a) A p-type a-Si:H layer,
 - (b) An intrinsic a-Si:H layer consisting of a first partial layer with more μ -tau product, a second partial layer with less μ -tau product than the first partial layer, and a third partial layer with less μ -tau product than the first and second partial layers,
 - (c) An n-type a-Si:H layer.
8. An image sensor according to claim 1, characterized in that the detector (4) is a light-sensitive MOS capacitor, especially a MOS varactor.
9. An image sensor according to claim 1, characterized in that the storage (3) is an analog storage.
10. An image sensor according to claim 9, characterized in that the storage (3) is a capacitor.

11. An image sensor according to claim 10, characterized in that the storage (3) is a MOS capacitor.
12. An image sensor according to claim 11, characterized in that the capacitor is a plate capacitor whose plate consists of polysilicon.
13. An image sensor according to claim 11, characterized in that the capacitor is designed as a DRAM capacitor.
14. An image sensor according to claim 11, characterized in that the storage is a non-volatile storage, especially an EPROM, EEPROM, FRAM, i.e. a ferroelectric RAM, or a flash memory element.
15. An image sensor according to claim 1, characterized in that the storage is a digital store that is assigned an analog-digital converter.
16. An image sensor according to one of the prior claims, characterized in that the storage (3) is operated using a multilevel digital approach in which numerous digital bits are represented in an amplitude-discretized analog signal.
17. An image sensor according to claim 16, characterized in that the storage (3) is assigned a reciprocal analog-digital converter that measures the time that the illumination-proportional photostream requires to recharge a capacitor a specific voltage difference.

18. An image sensor according to claim 1, characterized in that at least two storages (3) are laterally adjacent.
19. An image sensor according to claim 1, characterized in that at least two storages (3) are vertically integrated.
20. An image sensor according to claim 16, characterized in that the storage (3) is designed as an SRAM cell.
21. An image sensor according to claim 1, characterized in that the storage (3) is designed as a magnetic, optical, organic or biological storage cell.
22. An image sensor according to one of the prior claims, characterized in that the storage control (2) is on the surface of the carrier (1) designed as a CMOS substrate.
23. An image sensor according to claim 23, characterized in that the electrical storage (3) is in a layer between the carrier (1) and the detector (4), and the connection between the storage (3) and storage control (2) is provided by via holes (6).

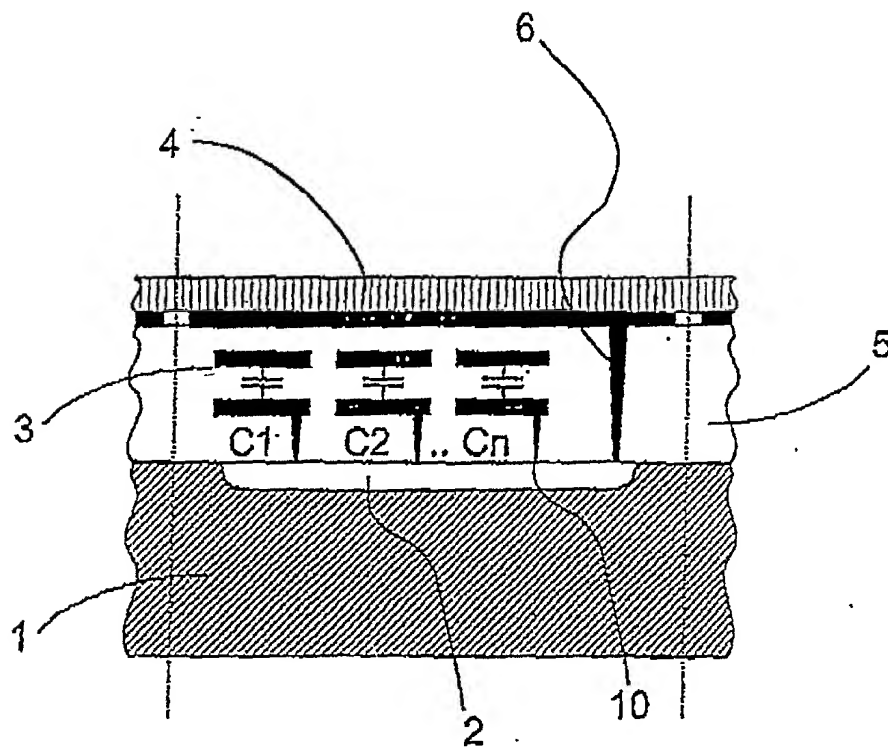


Fig. 1

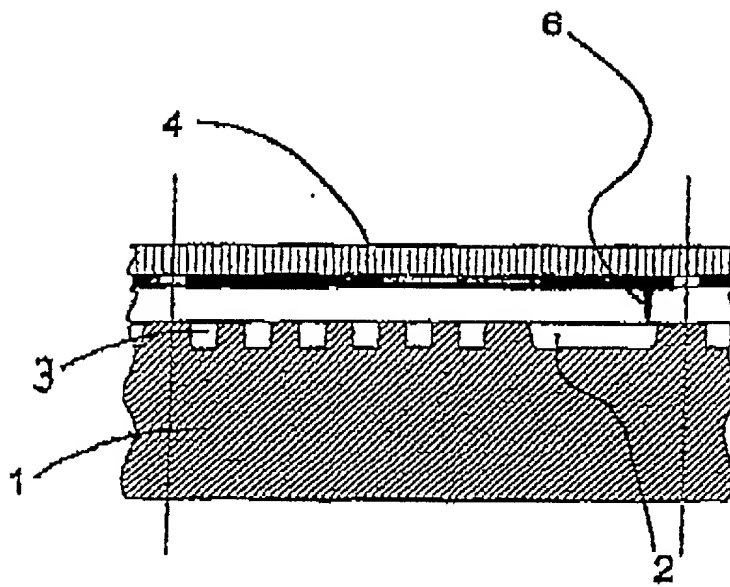


Fig. 2

3/4

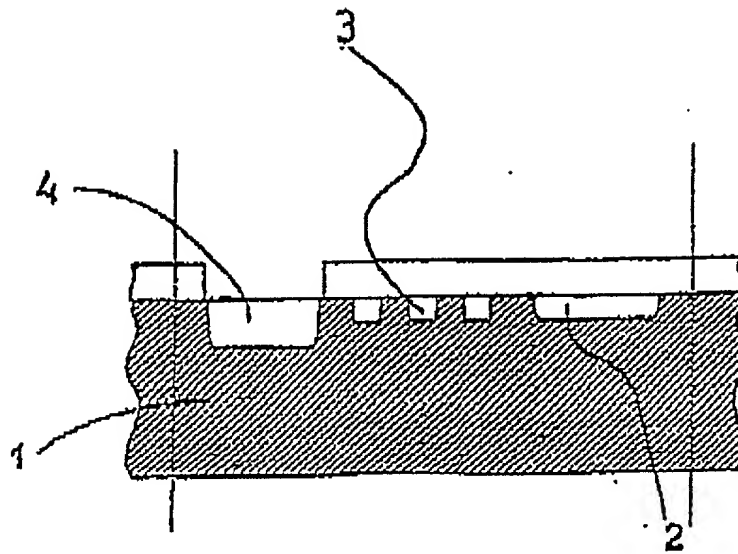


Fig. 3

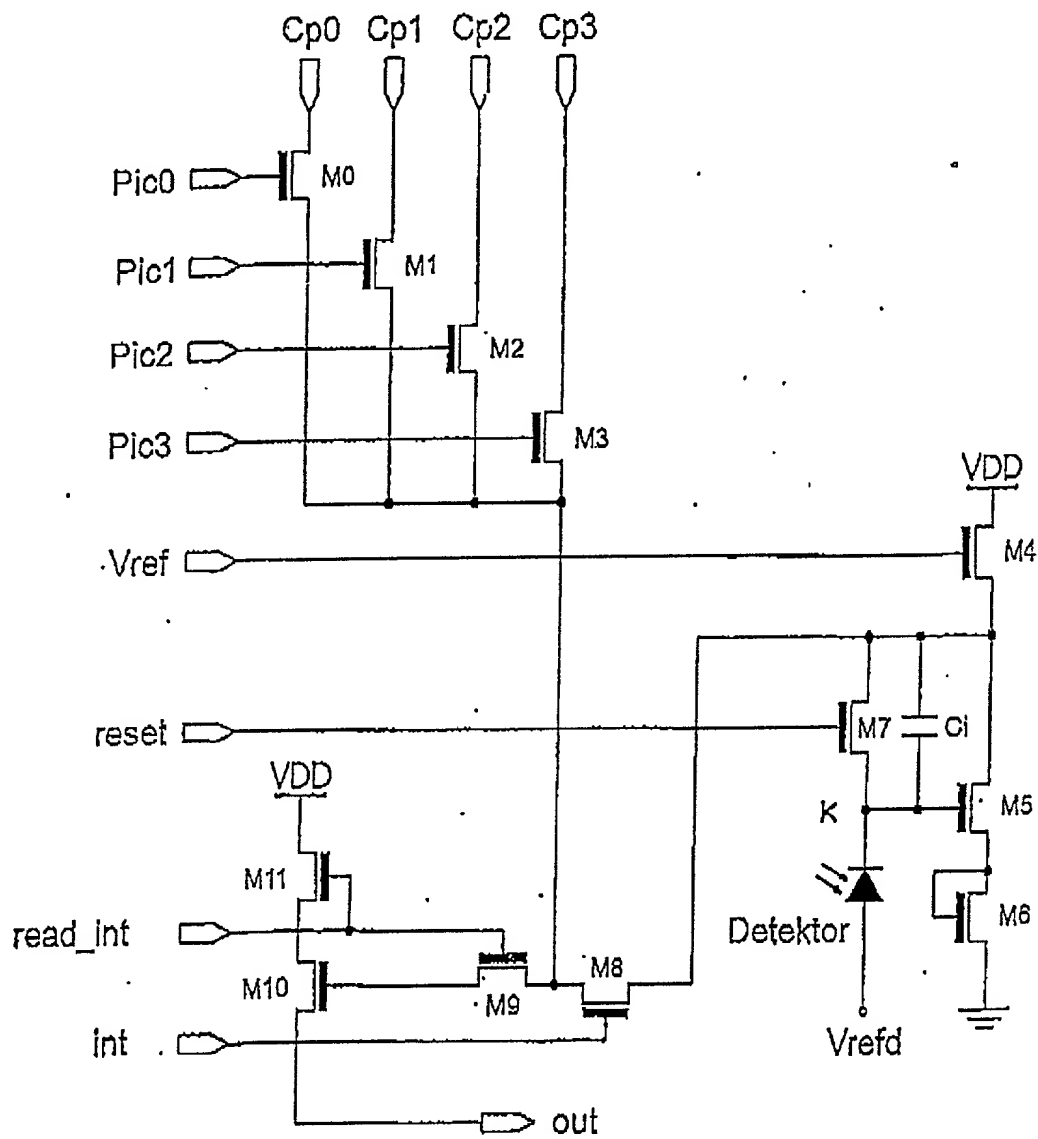


Fig. 4

212 969 2926

Attorney Docket No.: 20496-301

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMAGE SENSOR

the specification of which is attached hereto unless the following box is checked:

X was filed on March 1, 2000 as United States Application Number _____
or PCT International Application Number PCT/EP00/01705 and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified, by checking the box, any foreign application for patent or inventor's certificate, or PCT International Application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Not Claimed

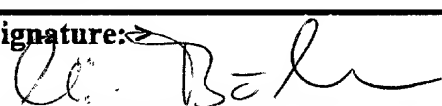
<u>199 09 550.7</u>	<u>Germany</u>	<u>4 March 1999</u>	_____
(Number)	(Country)	(Day/Month/Year Filed)	


_____	_____	_____	_____
(Number)	(Country)	(Day/Month/Year Filed)	

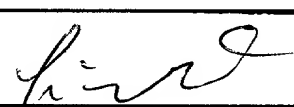
212 969 2926

Attorney Docket No. : 20496-301

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Attorney Docket No. : 20496-301

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application Number)

(Filing Date)

(Application Number)

(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

PCT/EP00/01705
(Application Number)

1 March 1999
(Filing Date)

Pending
(Status--patented,
pending, abandoned)

(Application Number)

(Filing Date)

(Status--patented,
pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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